

Appl. No. 10/708,640
Amdt. dated November 09, 2005
Reply to Office action of August 18, 2005

REMARKS/ARGUMENTS

1. *The specification has been checked to the extent necessary to determine the presence of possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may 5 become aware in the specification.*

Response:

10 The applicant has reviewed the specification as the examiner requested, however, no error was found. It is respectfully requested that the examiner precisely points out the where the minor error is. Reconsideration of the specification is politely requested.

15 2. *Claims 1-2 and 4-15 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,558,993 to Ohtani et al.*

Response:

20 Claim 1 has been amended to overcome the above rejection. Specifically, claim 1 now includes an additional limitation regarding a correlation among the gate length A, the channel region length B, and the lightly doped drains length C as following: $B+0.2C \leq 0.5A \leq B+0.8C$. The above limitation is included in order to further define the structural considerations given to the claimed invention.

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In lines 12-50, column 9, Ohtani teaches a thin-film transistor formed by patterning a semiconductor layer in a predetermined shape. The n-channel type thin-film transistor includes a channel forming region 104,

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an LDD region 108 adjacent to both sides of the channel forming region 104, and a first impurity region 109 functioned as the source or the drain region of the TFT and adjacent to the LDD region 108. Ohtani further discloses the LDD region 108 is divided into a part which overlaps the gate electrode 105 (gate-overlapped LDD region 108a) and a part which does not overlap the gate electrode 105 (non-gate-overlapped LDD region 108b).
5 However, Ohtani did not teach the correlation among the gate length A, the channel forming region length B, and the LDD region length C. Although the gate electrode length A and the gate-overlapped LDD regions length C is disclosed by Ohtani and the channel forming region length B can be inferred as $B=A-2C$ (according to Fig. 1A, the gate electrode 105 overlaps both sides of the gate-overlapped region 108a), the applicant would like to point out that it is not satisfied the correlation provided by the present application:
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15 The gate electrode length A: $0.1 \mu m < A < 10 \mu m$

The gate-overlapped LDD region length C: $0.1 \mu m < C < 2 \mu m$

$$B=A-2C = 0.1-2*0.1 = -0.1 < 0 \quad \text{or} \quad B=A-2C = 10-2*2 = 6$$

Therefore, the channel forming region length B: $0 \mu m < B < 6 \mu m$

20 If the widest electrode length A, the widest gate overlapped LDD regions C, and the widest channel forming length B are applied in the correlation $B+0.2C \leq 0.5A \leq B+0.8C$:

$$\cdot B+0.2C = 6+0.2*2 = 6.4$$

$$\cdot B+0.8C = 6+0.8*2 = 7.6$$

25 $\cdot 0.5A = 0.5*10 = 5$

Then, the correlation $B+0.2C \leq 0.5A \leq B+0.8C \leftrightarrow 6.4 < 5 < 7.6$

It is not satisfied

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Ohtani's teaching cannot satisfy the correlation in the claimed application, therefore the application asserts that the amended claim 1 is patentably distinct from Ohtani's disclosure. Reconsideration of the amended claim 1 is respectfully requested.

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Claims 2, 4-5, and 7-8 are dependent on claim 1 and should be allowed if claim 1 is allowed. Claim 6 is canceled.

Claim 9 recites a thin-film transistor comprising a substrate, a 10 semiconductor layer positioned on the substrate, the semiconductor layer comprising a channel region, two lightly doped drains, a source and a drain. The thin-film further comprises an insulating layer positioned on the semiconductor layer and a gate positioned on the insulating layer, the gate comprising a gate edge overlapped with the lightly doped drain adjacent 15 to the drain, the gate being not overlapped with the junction between the lightly doped drain, and the gate being not overlapped with the drain.

In general, the leakage currents are generated because a voltage 20 remains between the drain and the substrate when the transistor is during the off-operation, the leakage current problems are more sensitive around the drain. The applicant would like to point out that the leakage currents can be effectively reduced by overlapping a edge of the gate with the lightly adjacent to the drain, and preventing the edge of the gate from overlapping with either of the junction between the drain and 25 the lightly doped drain or drain. In addition, whether the gate overlaps with the lightly doped drain adjacent to the source and keeps away from the junction between the lightly doped drain and the source or not can be an optional design choice.

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Contrary to the present application, Ohtani's LDD regions 108 are all overlapped by the gate electrode 105 according to Figs 1-4. It is obvious that Ohtani did not consider that the leakage currents are more sensitive around the drain thus it can be effectively reduced by only overlapping the gate electrode with the LDD region adjacent to the drain. The applicant asserts that claim 9 is patentably distinct from Ohtani's disclosure, therefore reconsideration of claim 9 is politely requested.

10 Claims 10-11 are dependent on claim 9 and should be allowed if claim 9 is allowed.

15 Regarding claim 12, which recites the gate comprises a length A, the channel region comprises a length B, the lightly doped drain adjacent to the drain comprises a length C, and a correlation among these lengths is as following: $B+0.2C \leq 0.5A \leq B+0.8C$. As described above, the applicant believes that the lengths suggested by Ohtani do not satisfy the correlation provided by the present application:

The gate electrode length A: $0.1 \mu m < A < 10 \mu m$

20 The gate-overlapped LDD region length C: $0.1 \mu m < C < 2 \mu m$

$B = A - 2C = 0.1 - 2 * 0.1 = -0.1 < 0$ or $B = A - 2C = 10 - 2 * 2 = 6$

Therefore, the channel forming region length B: $0 \mu m < B < 6 \mu m$

25 If the widest electrode length A, the widest gate overlapped LDD regions C, and the widest channel forming length B are applied in the correlation $B+0.2C \leq 0.5A \leq B+0.8C$:

· $B+0.2C = 6+0.2*2 = 6.4$

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$$\cdot B + 0.8C = 6 + 0.8 \cdot 2 = 7.6$$

$$\cdot 0.5A = 0.5 \cdot 10 = 5$$

Then, the correlation $B + 0.2C \leq 0.5A \leq B + 0.8C \leftrightarrow 6.4 < 5 < 7.6$

It is not satisfied

5 Ohtani's teaching cannot satisfy the correlation in the claimed application, therefore the application asserts that the amended claim 1 is patentably distinct from Ohtani's disclosure. Reconsideration of claim 12 is respectfully requested.

10 In addition, claims 13-15 are dependent on claim 9 and should be allowed if claim 9 is allowed.

3. *Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,558,993 to Ohtani et al., in view of Yeh et al.*

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Response:

Claim 3 is dependent on claim 1 and should be allowed if claim 1 is allowed.

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Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

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Sincerely yours,

Winston Hsu

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